EAST SEARCH

9/19/2006

L#	Hits	Search String	Databases
S54	375	S30 or S32 or S35 or S46	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S38	40	S29 and ((instrument$3 or instrumentation) with (record$3 or identifY$3 or identified or identif	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S52	69	S29 and ((recursive or recursion) with (compil$3 or compilation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S36	7	S29 and (monitor$3 with (simulation near2 event))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S37	28	S29 and ((record$3 or identifY$3 or identified or identification) with (simulation near2 event))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S39	10	S29 and ((monitor$3 or record$3 or identifY$3 or identified or identification) with (logical near	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S34	73	S29 and (monitor$3 near2 (element or component or block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S35	171	S29 and (hierarchical$3 with (element or component or block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S31	53	S29 and ((instrument$3 or instrumentation) with (simulat$3 near2 model))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S30	109	S29 and (compil$3 with (simulat$3 near2 model))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S32	198	S29 and (hierarchical$3 near2 design)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S29	5054	((integrated or digital) near2 circuit) with simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S56	135	S53 and S55	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S57	302	S53 or S56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S40	0	S29 and ((compiled near2 file) with listing)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S42	44	S29 and ((instrument$3 or instrumentation) with (compil$3 or compilation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S43	82	S29 and ((instrument$3 or instrumentation) with (event or element or component or object))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S44	0	S29 and (compil$3 with (bill near2 material))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S45	7	S29 and (compil$3 with (output$3 near2 file))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S46	141	S29 and (("hardware description language" or HDL) near2 file)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S51	71	S29 and (parent near2 (element or component or object or block or entity))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S41	63	S29 and (compiled near2 file)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S49	7	S29 and (constraint with (data near2 structure))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S47	1183	S29 and (design with (element or component or object or block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S50	52	S29 and (incremental$2 near2 (compil$3 or compilation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S53	302	S31 or S34 or S36 or S37 or S38 or S39 or S41 or S42 or S43 or S45 or S49 or S50 or S51 c	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S55	273	S54 and S47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S58	5054	((integrated or digital) near2 circuit) with simulat$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S59	109	S58 and (compil$3 with (simulat$3 near2 model))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S60	53	S58 and ((instrument$3 or instrumentation) with (simulat$3 near2 model))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S61	198	S58 and (hierarchical$3 near2 design)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S62	73	S58 and (monitor$3 near2 (element or component or block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S63	171	S58 and (hierarchical$3 with (element or component or block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S65	28	S58 and ((record$3 or identifY$3 or identified or identification) with (simulation near2 event))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S64	7	S58 and (monitor$3 with (simulation near2 event))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S74	7	S58 and (constraint with (data near2 structure))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S75	52	S58 and (incremental$2 near2 (compil$3 or compilation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S66	40	S58 and ((instrument$3 or instrumentation) with (record$3 or identifY$3 or identified or identif	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S67	10	S58 and ((monitor$3 or record$3 or identifY$3 or identified or identification) with (logical near	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S68	63	S58 and (compiled near2 file)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S69	44	S58 and ((instrument$3 or instrumentation) with (compil$3 or compilation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

S70	82	S58 and ((instrument$3 or instrumentation) with (event or element or component or object))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S71	7	S58 and (compil$3 with (output$3 near2 file))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S72	141	S58 and (("hardware description language" or HDL) near2 file)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S73	1183	S58 and (design with (element or component or object or block))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S76	71	S58 and (parent near2 (element or component or object or block or entity))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S77	69	S58 and ((recursive or recursion) with (compil$3 or compilation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S78	302	S60 or S62 or S64 or S65 or S66 or S67 or S68 or S69 or S70 or S71 or S74 or S75 or S76 c	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S79	375	S59 or S61 or S63 or S72	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S81	135	S78 and S80	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S80	273	S79 and S73	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S82	302	S78 or S81	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

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9/19/2006

Results of search set S91:

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20060190910 A1	Method, system and program product providing a configuration specification language suppo	20060824	716/18	
US 20060190788 A1	METHOD AND APPARATUS FOR VERIFYING MEMORY TESTING SOFTWARE	20060824	714/733	
US 20060190239 A1	Method and system for hardware based reporting of assertion information for emulation and h	20060824	703/26	
US 20060149526 A1	Clock simulation system and method	20060706	703/16	
US 20060143524 A1	Built-in self-test emulator	20060629	714/30	
US 20060122818 A1	Method, system and program product for defining and recording threshold-qualified count eve	20060608	703/17	
US 20060117279 A1	Method for storing multiple levels of design data in a common database	20060601	716/4	
US 20060117274 A1	Behavior processor system and method	20060601	716/1	
US 20060089827 A1	Method, system and program product for defining and recording minium and maximum event	20060427	703/17	
US 20060089826 A1	Method, system and program product for defining and recording minimum and maximum cou	20060427	703/17	
US 20060080076 A1	System-level power estimation using heteregeneous power models	20060413	703/18	
US 20060031789 A1	Built-in self-test emulator	20060209	716/1	
US 20060026548 A1	Method, system and program product for providing a configuration specification language sup	20060202	716/18	
US 20060026478 A1	Built-in self-test emulator	20060202	714/733	
US 20060025978 A1	Method, system and program product supporting presentation of a simulated or hardware sys	20060202	703/14	
US 20060020442 A1	Built-in self-test emulator	20060126	703/28	
US 20060020411 A1	Built-in self-test emulator	20060126	702/117	
US 20060010409 A1	Semiconductor integrated circuit design method, design support system for the same, and de	20060112	716/6	
US 20060004556 A1	Method, system and program product for providing a configuration specification language sup	20060105	703/14	
US 20050278683 A1	Method, system and program product for specifying and using register entities to configure a	20051215	716/18	
US 20050251376 A1	Simulating operation of an electronic circuit	20051110	703/14	
US 20050248895 A1	System and method for determining thermal shutdown characteristics	20051110	361/103	
US 20050228630 A1	VCD-on-demand system and method	20051013	703/19	
US 20050162182 A1	Internally generating patterns for testing in an integrated circuit device	20050728	324/765	
US 20050149893 A1	Method, system and program product providing a configuration specification language having	20050707	716/4	
US 20050149883 A1	Method, system and program product providing a configuration specification language suppo	20050707	716/1	
US 20050149805 A1	Pending bug monitors for efficient processor development and debug	20050707	714/741	
US 20050149313 A1	Method and system for selective compilation of instrumentation entities into a simulation mod	20050707	703/22	

US 20050149309 A1	Method, system and program product supporting user tracing in a simulator	20050707	703/14
US 20050102645 A1	Method of generating a schematic driven layout for a hierarchical integrated circuit design	20050512	716/11
US 20050102572 A1	Memory debugger for system-on-a-chip designs	20050512	714/29
US 20050102125 A1	Inter-chip communication system	20050512	703/14
US 20050050509 A1	Method, system and program product providing a configuration specification language that su	20050303	716/18
US 20050049842 A1	Method, system and program product that automatically generate coverage instrumentation fo	20050303	703/14
US 20050049740 A1	Method, system and program product providing a configuration specification language having	20050303	700/121
US 20050036151 A1	Method and device for opically testing semiconductor elements	20050217	356/497
US 20050035785 A1	Logic circuit and semiconductor integrated circuit	20050217	326/104
US 20050027967 A1	Apparatus and method for two micro-operation flow using source override	20050203	712/216
US 20040267996 A1	Queued locks using monitor-memory wait	20041230	710/200
US 20040216080 A1	Method, system and program product for specifying and using dials having phased default va	20041028	716/18
US 20040216079 A1	Method, system and program product for specifying a configuration of a digital system descrit	20041028	716/18
US 20040216078 A1	Method, system and program product that utilize a configuration database to configure a hard	20041028	716/18
US 20040216077 A1	Method, system and program product for specifying and using a dial having a default value to	20041028	716/18
US 20040216076 A1	METHOD, SYSTEM AND PROGRAM PRODUCT FOR UTILIZING A CONFIGURATION DAT	20041028	716/18
US 20040216075 A1	Method, system and program product for specifying a dial group for a digital system describe	20041028	716/18
US 20040216068 A1	Method, system and program product for reducing a size of a configuration database utilized	20041028	716/11
US 20040216008 A1	Method, system and program product for automatically transforming a configuration of a digit	20041028	714/33
US 20040215436 A1	Method, system and program product for implementing a read-only dial in a configuration dat	20041028	703/15
US 20040215435 A1	Method, system and program product for determining a configuration of a digital design by ret	20041028	703/15
US 20040215434 A1	Method, system and program product for configuring a simulation model of a digital design	20041028	703/15
US 20040215433 A1	Method, system and program product that utilize a configuration database to configure a hard	20041028	703/14
US 20040215432 A1	Method, system and program product for specifying a configuration for multiple signal or dial i	20041028	703/14
US 20040204892 A1	Testing of integrated circuits from design documentation	20041014	702/117
US 20040193394 A1	Method for CPU simulation using virtual machine extensions	20040930	703/22
US 20040162805 A1	Method and system for automatically generating a global simulation model of an architecture	20040819	707/1
US 20040160239 A1	Integrated circuit early life failure detection by monitoring changes in current signatures	20040819	324/765
US 20040158803 A1	Integrated circuit, integrated circuit design method and hardware description generation meth	20040812	716/5
US 20040078767 A1	Representing the design of a sub-module in a hierarchical integrated circuit design and analy	20040422	716/8
US 20040060019 A1	METHOD AND APPARATUS FOR HIERARCHICAL CLOCK TREE ANALYSIS	20040325	716/6
US 20040025129 A1	System and methods for pre-artwork signal-timing verification of an integrated circuit design	20040205	716/6
US 20040015801 A1	Systems and methods for timing a linear data path element during signal-timing verification of	20040122	716/6
US 20040015338 A1	Method and apparatus for automated signal integrity checking	20040122	703/13
US 20040003360 A1	Systems and methods for time-budgeting a complex hierarchical integrated circuit	20040101	716/6
US 20030237078 A1	Incorporating simulation analysis instrumentation into HDL models	20031225	717/155
US 20030237067 A1	System and method for applying timing models in a static-timing analysis of a hierarchical inte	20031225	716/6
US 20030229482 A1	Apparatus and method for managing integrated circuit designs	20031211	703/14
US 20030217248 A1	Method and system for instruction-set architecture simulation using just in time compilation	20031120	712/208
US 20030191869 A1	C-API instrumentation for HDL models	20031009	719/328
US 20030191621 A1	Method and system for reducing storage and transmission requirements for simulation results	20031009	703/17
US 20030191620 A1	Dynamic loading of C-API HDL model instrumentation	20031009	703/17
US 20030191618 A1	Method and system for reducing storage requirements of simulation data via keyword restricti	20031009	703/13
US 20030191617 A1	Method and system for selectively storing and retrieving simulation data utilizing keywords	20031009	703/13
US 20030144828 A1	Hub array system and method	20030731	703/21
US 20030135838 A1	Method and apparatus for isolating the root of indeterminate logic values in an HDL simulatio	20030717	716/18
US 20030135354 A1	Tracking coverage results in a batch simulation farm network	20030717	703/13
US 20030126379 A1	Instruction sequences for suspending execution of a thread until a specified memory access o	20030703	711/150

US 20030126375 A1	Coherency techniques for suspending execution of a thread until a specified memory access	20030703	711/145
US 20030126186 A1	Method and apparatus for suspending execution of a thread until a specified memory access	20030703	718/107
US 20030125915 A1	Count data access in a distributed simulation environment	20030703	703/13
US 20030101382 A1	Fail thresholding in a batch simulation farm network	20030529	714/39
US 20030101041 A1	Annealing harvest event testcase collection within a batch simulation farm	20030529	703/22
US 20030101039 A1	Maintaining data integrity within a distributed simulation environment	20030529	703/16
US 20030101038 A1	Centralized disablement of instrumentation events within a batch simulation farm network	20030529	703/16
US 20030101035 A1	Non-redundant collection of harvest events within a batch simulation farm network	20030529	703/13
US 20030093764 A1	Automated system-on-chip integrated circuit design verification system	20030515	716/5
US 20030061580 A1	Simulation method and compiler for hardware/software programming	20030327	716/4
US 20030009734 A1	Method for generating design constraints for modules in a hierarchical integrated circuit desig	20030109	716/6
US 20020188922 A1	Method for storing multiple levels of design data in a common database	20021212	716/18
US 20020188916 A1	Integrated circuit, integrated circuit design method and hardware description generation meth	20021212	716/4
US 20020183054 A1	Mobile system testing architecture	20021205	455/423
US 20020152456 A1	Software and hardware simulation	20021017	717/135
US 20020152060 A1	Inter-chip communication system	20021017	703/17
US 20020138814 A1	Virtual component having a detachable verification-supporting circuit, a method of verifying th	20020926	716/5
US 20020133325 A1	Discrete event simulator	20020919	703/17
US 20020128809 A1	Randomized simulation model instrumentation	20020912	703/17
US 20020124085 A1	Method of simulating operation of logical unit, and computer-readable recording medium reta	20020905	709/226
US 20020123875 A1	Hierarchical processing of simulation model events	20020905	703/17
US 20020123874 A1	Detecting events within simulation models	20020905	703/17
US 20020123873 A1	Signal override for simulation models	20020905	703/17
US 20020120922 A1	Embedded hardware description language instrumentation	20020829	717/143
US 20020073375 A1	Method and apparatus for test generation during circuit design	20020613	714/739
US 20020052725 A1	Distributed simulation	20020502	703/22
US 20020049577 A1	Current coupling for mixed circuit simulation	20020425	703/14
US 20020032559 A1	Hardware and software co-simulation including executing an analyzed user program	20020314	703/22
US 20020023252 A1	METHOD FOR INCREMENTAL TIMING ANALYSIS	20020221	716/6
US 20020019969 A1	Hardware and software co-simulation including simulating the cache of a target processor	20020214	716/5
US 20020011606 A1	Semiconductor integrated circuit and designing method thereof	20020131	257/200
US 20010012014 A1	SINGLE LOGICAL IN X WINDOWS WITH DIRECT HARDWARE ACCESS TO THE FRAME	20010809	345/541
US 20010011212 A1	METHOD AND APPARATUS FOR GATE-LEVEL SIMULATION OF SYNTHESIZED REGIST	20010802	703/22
US 7107569 B2	Design method and apparatus for a semiconductor integrated circuit comprising checkers ver	20060912	716/18
US 7103863 B2	Representing the design of a sub-module in a hierarchical integrated circuit design and analy	20060905	716/7
US 7098696 B2	Logic circuit and semiconductor integrated circuit	20060829	326/99
US 7096434 B2	Method, system and program product providing a configuration specification language suppo	20060822	716/1
US 7092868 B2	Annealing harvest event testcase collection within a batch simulation farm	20060815	703/22
US 7092864 B2	Signal override for simulation models	20060815	703/14
US 7085703 B2	Count data access in a distributed simulation environment	20060801	703/17
US 7082589 B2	Method of generating a schematic driven layout for a hierarchical integrated circuit design	20060725	716/11
US 7080347 B2	Method, system and program product for specifying a configuration of a digital system descrit	20060718	716/18
US 7080346 B2	Method, system and program product for automatically transforming a configuration of a digit	20060718	716/18
US 7076410 B1	Method and apparatus for efficiently viewing a number of selected components using a datab	20060711	703/6
US 7062746 B2	Method, system and program product that utilize a configuration database to configure a hard	20060613	716/18
US 7062745 B2	Method, system and program product for specifying and using a dial having a default value to	20060613	716/18
US 7047507 B2	System and method for determining wire capacitance for a VLSI circuit	20060516	716/5
US 7039894 B2	Method, system and program product for specifying and using dials having phased default va	20060502	716/18

US 7039574 B1	Naming and managing simulation model events	20060502	703/17
US 7035781 B1	Mixed language simulator	20060425	703/14
US 7027971 B2	Centralized disablement of instrumentation events within a batch simulation farm network	20060411	703/14
US 6993736 B2	Pending bug monitors for efficient processor development and debug	20060131	716/4
US 6993729 B2	Method, system and program product for specifying a dial group for a digital system describe	20060131	716/1
US 6988253 B1	Methods, apparatus and computer program products that perform layout versus schematic cc	20060117	716/5
US 6985840 B1	Circuit property verification system	20060110	703/7
US 6978231 B2	Embedded hardware description language instrumentation	20051220	703/14
US 6978216 B2	Testing of integrated circuits from design documentation	20051220	702/118
US 6954915 B2	System and methods for pre-artwork signal-timing verification of an integrated circuit design	20051011	716/6
US 6941527 B2	Method, system and program product for reducing a size of a configuration database utilized	20050906	716/2
US 6941257 B2	Hierarchical processing of simulation model events	20050906	703/15
US 6934885 B2	Fail thresholding in a batch simulation farm network	20050823	714/33
US 6925621 B2	System and method for applying timing models in a static-timing analysis of a hierarchical inte	20050802	716/6
US 6920418 B2	Detecting events within simulation models	20050719	703/17
US 6910200 B1	Method and apparatus for associating selected circuit instances and for performing a group o	20050621	716/9
US 6910194 B2	Systems and methods for timing a linear data path element during signal-timing verification o	20050621	716/6
US 6879949 B2	Current coupling for mixed circuit simulation	20050412	703/14
US 6873171 B2	Integrated circuit early life failure detection by monitoring changes in current signatures	20050329	324/765
US 6862563 B1	Method and apparatus for managing the configuration and functionality of a semiconductor d	20050301	703/14
US 6845494 B2	Method for generating design constraints for modules in a hierarchical integrated circuit desig	20050118	716/6
US 6836874 B2	Systems and methods for time-budgeting a complex hierarchical integrated circuit	20041228	716/6
US 6826732 B2	Method, system and program product for utilizing a configuration database to configure a har	20041130	716/1
US 6810507 B2	Method and apparatus for isolating the root of indeterminate logic values in an HDL simulatio	20041026	716/4
US 6810442 B1	Memory mapping system and method	20041026	710/22
US 6799307 B1	Layout versus schematic (LVS) comparison tools that use advanced symmetry resolution tech	20040928	716/5
US 6792379 B2	Data-based control of integrated circuits	20040914	702/130
US 6785873 B1	Emulation system with multiple asynchronous clocks	20040831	716/4
US 6754763 B2	Multi-board connection system for use in electronic design automation	20040622	710/317
US 6751583 B1	Hardware and software co-simulation including simulating a target processor using binary tra	20040615	703/17
US 6714032 B1	Integrated circuit early life failure detection by monitoring changes in current signatures	20040330	324/765
US 6708322 B2	Integrated circuit, integrated circuit design method and hardware description generation meth	20040316	716/18
US 6687889 B1	Method and apparatus for hierarchical clock tree analysis	20040203	716/6
US 6684376 B1	Method and apparatus for selecting components within a circuit design database	20040127	716/8
US 6658633 B2	Automated system-on-chip integrated circuit design verification system	20031202	716/5
US 6651225 B1	Dynamic evaluation logic system and method	20031118	716/4
US 6606734 B2	Simulation method and compiler for hardware/software programming	20030812	716/4
US 6600181 B2	Semiconductor integrated circuit and designing method thereof	20030729	257/277
US 6587995 B1	Enhanced programmable core model with integrated graphical debugging functionality	20030701	716/4
US 6584436 B2	Hardware and software co-simulation including executing an analyzed user program	20030624	703/13
US 6530054 B2	Method and apparatus for test generation during circuit design	20030304	714/739
US 6516456 B1	Method and apparatus for selectively viewing nets within a database editor tool	20030204	716/8
US 6505328 B1	Method for storing multiple levels of design data in a common database	20030107	716/7
US 6505323 B1	Methods, apparatus and computer program products that perform layout versus schematic cc	20030107	716/3
US 6499130 B1	Methods, apparatus and computer program products that perform layout versus schematic cc	20021224	716/5
US 6493864 B1	Integrated circuit block model representation hierarchical handling of timing exceptions	20021210	716/18
US 6487699 B1	Method of controlling external models in system-on-chip verification	20021126	716/4
US 6470482 B1	METHOD AND SYSTEM FOR CREATING, DERIVING AND VALIDATING STRUCTURAL DE	20021022	716/6

US 6470478 B1	Method and system for counting events within a simulation model	20021022	716/4
US 6466898 B1	Multithreaded, mixed hardware description languages logic simulation on engineering workst	20021015	703/17
US 6449750 B1	Design verification device, method and memory media for integrated circuits	20020910	716/4
US 6429728 B1	Component assisted power regulation	20020806	327/540
US 6421251 B1	Array board interconnect system and method	20020716	361/788
US 6417849 B2	Single logical screen in X windows with direct hardware access to the frame buffer for 3D ren	20020709	345/419
US 6389379 B1	Converification system and method	20020514	703/14
US 6367056 B1	Method for incremental timing analysis	20020402	716/5
US 6350943 B1	Electric instrument amplifier	20020226	84/603
US 6347388 B1	Method and apparatus for test generation during circuit design	20020212	714/739
US 6336087 B1	Method and apparatus for gate-level simulation of synthesized register transfer level design w	20020101	703/15
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120	716/6
US 6321186 B1	Method and apparatus for integrated circuit design verification	20011120	703/15
US 6263302 B1	Hardware and software co-simulation including simulating the cache of a target processor	20010717	703/17
US 6263301 B1	Method and apparatus for storing and viewing data generated from a computer simulation of	20010717	703/14
US 6240376 B1	Method and apparatus for gate-level simulation of synthesized register transfer level designs	20010529	703/15
US 6230114 B1	Hardware and software co-simulation including executing an analyzed user program	20010508	703/13
US 6230084 B1	Vehicle characteristic change system and method	20010508	701/1
US 6223142 B1	Method and system for incrementally compiling instrumentation into a simulation model	20010424	703/15
US 6212491 B1	Automatic adjustment for counting instrumentation	20010403	703/14
US 6205567 B1	Fault simulation method and apparatus, and storage medium storing fault simulation program	20010320	714/741
US 6205374 B1	Vehicle characteristic change system and method	20010320	701/1
US 6202198 B1	Programmable integrated analog input/output circuit with distributed matching memory array	20010313	716/17
US 6202042 B1	Hardware simulator instrumentation	20010313	703/16
US 6195776 B1	Method and system for transforming scan-based sequential circuits with multiple skewed capt	20010227	714/738
US 6195629 B1	Method and system for selectively disabling simulation model instrumentation	20010227	703/17
US 6195627 B1	Method and system for instrumenting simulation models	20010227	703/14
US 6189131 B1	Method of selecting and synthesizing metal interconnect wires in integrated circuits	20010213	716/8
US 6182258 B1	Method and apparatus for test generation during circuit design	20010130	714/739
US 6173241 B1	Logic simulator which can maintain, store, and use historical event records	20010109	703/13
US 6169992 B1	Search engine for remote access to database management systems	20010102	707/103R
US 6163763 A	Method and apparatus for recording and viewing error data generated from a computer simul	20001219	703/17
US 6134516 A	Simulation server system and method	20001017	703/27
US 6087967 A	Method for generating and reading a compressed all event trace file	20000711	341/63
US 6061176 A	Microscope system for observation and display of microcirculation at multiple body areas	20000509	359/368
US 6026230 A	Memory simulation system and method	20000215	703/13
US 6021271 A	Methods of simulating an electronic circuit design	20000201	703/14
US 6009531 A	Transition analysis and circuit resynthesis method and device for digital circuit modeling	19991228	713/400
US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 6002861 A	Method for performing simulation using a hardware emulation system	19991214	703/16
US 5987239 A	Computer system and method for building a hardware description language representation of	19991116	716/1
US 5960171 A	Dynamic signal loop resolution in a compiled cycle based circuit simulator	19990928	714/49
US 5940604 A	Method and apparatus for monitoring the performance of a circuit optimization tool	19990817	716/2
US 5920490 A	Integrated circuit test stimulus verification and vector extraction system	19990706	716/2
US 5910903 A	Method and apparatus for verifying, analyzing and optimizing a distributed simulation	19990608	703/6
US 5907698 A	Method and apparatus for characterizing static and dynamic operation of an architectural syst	19990525	716/6
US 5867399 A	System and method for creating and validating structural description of electronic system fron	19990202	716/18
US 5838949 A	System and method for execution-sequenced processing of electronic design simulation resu	19981117	703/13

US 5825658 A	Method and a system for specifying and automatically analyzing multiple clock timing constrai	19981020	716/6
US 5821788 A	Zero consumption power-on-reset	19981013	327/143
US 5812414 A	Method for performing simulation using a hardware logic emulation system	19980922	716/16
US 5805862 A	Method of forming an integrated circuit	19980908	703/15
US 5801958 A	Method and system for creating and validating low level description of electronic design from	19980901	716/18
US 5796623 A	Apparatus and method for performing computations with electrically reconfigurable logic devi	19980818	703/23
US 5781718 A	Method for generating test pattern sets during a functional simulation and apparatus	19980714	714/33
US 5757672 A	Monitoring system and technique	19980526	702/116
US 5752002 A	Method and apparatus for performance optimization of integrated circuit designs	19980512	703/14
US 5734581 A	Method for implementing tri-state nets in a logic emulation system	19980331	703/15
US 5729466 A	Optimization multiple performance criteria by simulating the behavior of a constraint graph ex	19980317	716/10
US 5686855 A	Process monitor for CMOS integrated circuits	19971111	327/378
US 5675728 A	Apparatus and method identifying false timing paths in digital circuits	19971007	714/28
US 5661662 A	Structures and methods for adding stimulus and response functions to a circuit design under	19970826	716/16
US 5657241 A	Routing methods for use in a logic emulation system	19970812	716/16
US 5650946 A	Logic simulator which can maintain, store and use historical event records	19970722	703/16
US 5650938 A	Method and apparatus for verifying asynchronous circuits using static timing analysis and dyn	19970722	716/6
US 5649176 A	Transition analysis and circuit resynthesis method and device for digital circuit modeling	19970715	713/400
US 5636132 A	Method and apparatus for constraining the compaction of components of a circuit layout	19970603	716/2
US 5631596 A	Process monitor for CMOS integrated circuits	19970520	327/378
US 5623418 A	System and method for creating and validating structural description of electronic system	19970422	716/1
US 5619683 A	Reference international card harmonization coupler	19970408	710/62
US 5612891 A	Hardware logic emulation system with memory capability	19970318	716/16
US 5604895 A	Method and apparatus for inserting computer code into a high level language (HLL) software	19970218	703/13
US 5555201 A	Method and system for creating and validating low level description of electronic design from	19960910	716/1
US H001590 H	Portable aircraft instrumentation data simulator	19960903	703/16
US 5544067 A	Method and system for creating, deriving and validating structural description of electronic sy	19960806	703/14
US 5526517 A	Concurrently operating design tools in an electronic computer aided design system	19960611	707/8
US 5517506 A	Method and data processing system for testing circuits using boolean differences	19960514	714/744
US 5515384 A	Method and system of fault diagnosis of application specific electronic circuits	19960507	714/732
US 5512703 A	Electronic musical instrument utilizing a tone generator of a delayed feedback type controllab	19960430	84/600
US 5497331 A	Semiconductor integrated circuit device fabrication method and its fabrication apparatus	19960305	700/121
US 5495180 A	DC biasing and AC loading of high gain frequency transistors	19960227	324/765
US 5490783 A	Flight simulator having active electronic display controls	19960213	434/35
US 5486786 A	Process monitor for CMOS integrated circuits	19960123	327/378
US 5452231 A	Hierarchically connected reconfigurable logic assembly	19950919	716/16
US 5448496 A	Partial crossbar interconnect architecture for reconfigurably connecting multiple reprogramma	19950905	716/16
US 5437037 A	Simulation using compiled function description language	19950725	717/146
US 5384720 A	Logic circuit simulator and logic simulation method having reduced number of simulation evel	19950124	703/16
US 5383167 A	Method and apparatus for histogram based digital circuit simulator	19950117	703/19
US 5325309 A	Method and apparatus for integrated circuit diagnosis	19940628	703/15
US 5274570 A	Integrated circuit having metal substrate	19931228	716/1
US 5051938 A	Simulation of selected logic circuit designs	19910924	703/15
US 5036479 A	Modular automated avionics test system	19910730	702/121
US 5036473 A	Method of using electronically reconfigurable logic circuits	19910730	703/23
US 4878179 A	Interactive diagnostic methodology and apparatus for microelectronic devices	19891031	716/4
US 4827427 A	Instantaneous incremental compiler for producing logic circuit designs	19890502	703/14
US 4725971 A	Digital system simulation method and apparatus	19880216	703/14

US 4719834 A	Enhanced characteristics musical instrument	19880119	84/652
US 4695968 A	Digital system simulation method and apparatus having improved sampling	19870922	703/13
US 4646255 A	Gyro simulator	19870224	703/8
US 4630517 A	Sharing sound-producing channels in an accompaniment-type musical instrument	19861223	84/613
US 4628471 A	Digital system simulation method and apparatus having two signal-level modes of operation	19861209	703/14
US 4543526 A	Capacitive device for the measurement of displacements	19850924	324/725
US 4489220 A	Test set	19841218	379/27.01
US 4476765 A	Electronic music signal generator	19841016	84/604
US 4426904 A	Envelope control for electronic musical instrument	19840124	84/627
US 4141269 A	Electronic musical instrument	19790227	84/687
US 4108040 A	Electronic musical instrument	19780822	84/608
US 4088900 A	Safety circuit, especially for elevators and the like	19780509	307/149
US 4067253 A	Electronic tone-generating system	19780110	84/687
US 4045736 A	Method for composing electrical test patterns for testing AC parameters in integrated circuits	19770830	714/741
US 3902393 A	Automatic rhythm control circuit for musical instrument accompaniment	19750902	84/668
US 3585891 A	AN ELECTRONIC RHYTHM GENERATOR PARTICULARLY SUITABLE FOR INTEGRATED	19710622	84/667
US 3585599 A	UNIVERSAL SYSTEM SERVICE ADAPTER	19710615	714/45
DE 10031536 A1	Results based semiconductor testing system for use in the electronic development automatio	20010118	
US 6687889 B	Clock skew analysis method for hierarchical clock tree in integrated circuit, involves determini	20040203	
US 20030101382 A	Fail event tracking method for use in digital circuit simulation, involves receiving fail event pac	20030529	
US 6470478 B	Event counting method for simulation of digital circuit design, involves generating linear feedt	20021022	
US 20020128809 A	Digital circuit design testing program storage medium for ECAD systems, has data fields inclu	20020912	
US 20020123875 A	Computer readable recorded medium storing digital circuit designing and simulating program	20020905	
US 20020040457 A	Test data generation method for testing integrated circuit, involves determining multiple analy	20020404	
US 6223142 B	Method for compiling instrumentation logic into simulation model of digital circuit design, invol	20010424	
US 6212491 B	Counting rate adjusting method involves including design entity sequenced in accordance wit	20010403	
US 6202042 B	Logical failure detection for hardware accelerated simulation model of digital circuit, by model	20010313	
US 6195629 B	Instrumentation entity output disabling method involves masking output signal selectively by c	20010227	
US 6195627 B	Computer aided design and verification for simulating digital circuit design model, involves uti	20010227	
DE 10031536 A	Results based semiconductor testing system for use in the electronic development automatio	20010118	
US 6173241 B	Circuit operation event driven simulation recording method involves recording new events in e	20010109	
KR 2000017147 A	Application specific integrated circuit designing method for configuring microprocessor core e	20000325	
EP 697668 A	Identification method for false timing paths in digital circuit - involves identifying each path an	19960221	
DE 3221447 C	Providing accompaniment to electronic musical instrument - mapping preselected number of	19861223	